PUBLICATIONS 2004

Electronic Devices

1. S. Andersson, and C. Svensson, "An Active Recursive RF Filter in 0.35 μm BiCMOS" has been accepted for publication in the journal Analog Integrated Circuits and Signal Processing.
2. D. Jakonis, K. Folkesson, J. Dabrowski, P. Eriksson, C. Svensson: ”A 2.4-GHz RF sampling receiver front-end in 0.18μm CMOS”, submited to IEEE Journal of Solid-State.
3. C. Svensson: ”Forskning ska ha tillväxt som mål”, in Ny Teknik 2004-03-10.
4. C. Svensson: ”Forskning måste ha tillväxt som mål”, in Dagens Industri 2004-01-24, p 3.
5. S. Andersson, and C. Svensson, “Channel length as a design parameter for low noise wideband LNAs in deep submicron CMOS technologies, in Proc. of 22nd Norchip Conference, pp. 123-126, Oslo, Norway, 8-9 November 2004.
6. H. Bengtson, C. Svensson, "Amplifier stability related to power supply impedance," in Proc.of The 11th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES), pp. 151-156, Szczecin, Poland, 24-26 June 2004.
7. H. Bengtson, C. Svensson, "2.5 Gb/s, 72 Ω, transimpedance amplifier in 0.35 μm CMOS, " in Proc. of the 2004 IEEE 7th International Analog VLSI Workshop (AVLSIWS), pp. 261-266, Macau, 13-15 Oct. 2004.
8. H. Bengtson, C. Svensson, "A scalable and robust rail-to-rail delay cell for DLLs," in Proc.of the IEEE International SOC Conference, pp. 135-136, Santa Clara, USA, 12-15 Sept. 2004.
9. P. Caputa, A. Alvandpour, C. Svensson, ”High-speed on-chip interconnect modeling for circuit simulation”, in Proc. of 22nd Norchip Conference, pp. 143-146, Oslo, Norway, 8-9 November 2004.
10. P. Caputa, M. A. Anders, C. Svensson, R. K. Krishnamurthy, and S. Borkar, "A Low-swing Single-ended L1 Cache Bus Technique for Sub-90nm Technologies", in Proc. of ESSCIRC, pp. 475-477, Leuven, Belgium, 21-23 Sept. 2004.
11. P. Caputa, H. Fredriksson, M.Hansson, S. Andersson, A. Alvandpour, and C.Svensson, "An Extended Transition Energy Cost Model for Buses in Deep Submicron Technologies", in Proc. of The Forteenth International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2004, pp. 849-858, Santorini, Greece, September 15-17 2004.
12. I. Carlson, S. Andersson, S. Natarajan, A. Alvandpour, “A high density, low leakage, 5T SRAM for embedded caches”, in proceedings of European Solid-State Circuits Conference, ESSCIRC, pp. 215-222, Leuven, Belgium, September 21-23 2004.
13. J. Dabrowski, L .Li, “Signal Path Sensitization for Built-in-Self-Test in Integrated RF Transceivers”, in Proc of DDECS’04, pp. 59-66, Stara Lesna, Slovakia, 19-21 April 2004.

14. J. Dabrowski, “Fault Modeling of RF Blocks Based on Noise Analysis”, in Proc. of ISCAS’04, pp. I-513-516, Vancouver, Canada, 24-26 May 2004.

15. J. Dąbrowski, J. Gonzalez Bayon, “Mixed Loopback BiST for RF Digital Transceivers”, in Proc. of DFT’04, pp. 200-288, Cannes, France, 11-13 Oct. 2004.

16. A. Edman, and C. Svensson, “Timing closure through a globally synchronous, timing partitioned design methodology”, in Proc. of 41sr Design Automation Conference, pp. 71-74, San Diego, USA, 7-11 June 2004.

17. K. Folkesson, D. Jakonis, J. Dabrowski, Ch. Svensson, "Design of RF sampling receiver front-end", in Proceedings of MIXDES 2004, pp. 538-543, Szcecin, Poland, 2004. **Outstanding paper Award.**

18. K. Folkesson, and C. Svensson, "Robust Multi-Phase Clock Generation with Reduced Jitter", in Proc. of SOCC, pp. 167-168, Santa Clara, USA, 12-15 Sept 2004.

19. H. Fredriksson, and C. Svensson,"Mixed-signal decision feedback equalizer for multi-drop, Gb/s, memory buses, a feasibility study", in proceedings of SOCC, pp. 147-148, Santa Clara, 13-15 Sept. 2004.

20. M. Hansson, and A. Alvandpour, "A Low Clock Load Conditional Flip-flop", in Proc. of IEEE International System-on-Chip Conference, SoCC, pp. 169-170, Santa Clara, USA, 12-15 September 2004.

21. D. Jakonis, K. Folkesson, C. Svensson, J. Dabrowski, P. Eriksson, "An RF sampling downconversion filter for a receiver front-end", in Proceedings of MWSCAS, pp. I-165-I-168, Hiroshima, Japan, 2004.

22. L. Lindgren, "Elimination of Quantization Effects in Measured Temporal Noise", in Proceedings of 2004 IEEE International Symposium on Circuits and System (ISCAS04), Vancouver, volume IV, pp. IV-932-935, May 23-26 2004, **Received the Sensory Systems Track Best Paper Award.**

23. R. Malmqvist, M. Hansson, C. Samuelsson, et. al, "Some Important Aspects on the Design of Active Microwave Filters using Standard RF Silicon Process Technologies", European Microwave Conference, EuMC 2004, pp. 941-944, Amsterdam, The Netherlands, 12-14 Oct. 2004.

24. B. Mesgarzadeh, C. Svensson, A. Alvandpour, "A New Mesochronous Clocking Scheme for Synchronization in SoC", in Proc. of IEEE Symp. on Circuits and Systems (ISCAS'04), pp. II -605-608, Vancouver, Canada, 23-26 May 2004.

25. B. Mesgarzadeh, "A CMOS Implementation of Min-Max Circuits in Current mode and A Sample Fuzzy Application", IEEE International Conf. on Fuzzy Systems, p. 170, Budapest, Hungary, 25-29 July 2004.

26. S. Natarajan, A. Alvandpour, (invited paper), “Mainstream Memory Technologies in Deep Submicron”, in Proceeding of the 12th IEEE Mediterranean Electrotechnical Conference, MELECON, pp. 175-178, Dubrovnik, Croatia, 12-15 May 2004.

27. H. Ohlsson, B. Mesgarzadeh, K. Johansson, O. Gustafsson, P. Löwenborg, H. Johansson, A. Alvandpour, “A 16 GSPS 0.18 μm CMOS decimator for single-bit ∑Δ-modulation”, in Proc. of 22nd Norchip Conference, pp. 175-178, Oslo, Norway, 8-9 November 2004.

28. Svensson, (invited paper), “Synchronous latency insensitive design”, in Proc. of 10th IEEE International Symposium on Asynchronous Circuits and Systems, p. 3, Crete, Greece, 19-23 April 2004.

29. M. Andersson, J. Elbornsson, J-E Eklund, J. Alvebrant, H. Fredriksson, ”Verification of a blind mismatch error equalization method for randomly interleaved ADCs using a 2.5 V/12b/30MSs PSAADC”, in Proc. Of SSOC 2004, 4 p., Båstad, 13-14 April, 2004.

30. S. Andersson, Ch. Svensson, "Channel length as a design parameter for low noise wideband LNA’s in deep submicron CMOS technologies", Swedish System-on-Chip Conference, SSoCC 2004, 4 p., Båstad, Sweden, April 13-14 2004.

31. P. Caputa, A. Alvandpour, and Ch.Svensson, in Proc. of "High-speed on-chip interconnect modeling for circuit simulation", Swedish System-on-Chip Conference, Båstad, 4 p.,13-14 April 2004.

32. K. Folkesson, D. Jakonis, J. Dabrowski, Ch. Svensson, "RF-sampling receiver front-end design", in Proceedings of SSoCC'04, 4 p., Båstad, Sweden, 13-14 April 2004.

33. H. Fredriksson, Ch. Svensson, "Gb/s equalizer for multi-drop memory buses", in Proc of SSoCC 2004, 4 p., Båstad, Sweden, April 13-14 2004.

34. M. Hansson, and A. Alvandpour, "A Leakage Compensation Technique for Low-Power Dynamic Latches", in Proc. of Swedish System-on-Chip Conference, SSoCC 2004,4 p., Båstad, Sweden, April 13-14 2004.

35. Håkan Bengtson, “High speed CMOS optical receiver”, Linköping University, Dissertation No. 904, ISBN91-85295-61-2, ISSN 0345-7524, 2004.

36. Kalle Folkesson, “ADC modeling from a system perspective and design of RF-sampling radio receivers”, Linköping University Dissertation No. 911, ISBN 91-85295-88-4, ISSN 0345-7524, 2004.

37. Darius Jakonis, “Direct RF sampling receivers for wireless systems in CMOS technology”, Linköping University, Dissertation No. 881, ISBN 91-737-965-0, ISSN 0345-7524, 2004.

38. Stefan Andersson, “New directions in RF LNA design”, Linköping University, Thesis No. 1101, LiU-TEK-LIC-2004:30.

39. Peter Caputa, “Design of efficient high-speed on-chip global interconnects”.Linköing University, Thesis No. 1136, LiU-TEK-LIC-2004:65.

40. Christer Svensson, “Low-Power and Low-Voltage Communication for SOC´s”, in C. Piguet, ed. Low-Power Electronics Design, CRC-Press, 2004.

41. Atila Alvandpour, "High-performance and Low-voltage Datapath and Interconnect Design Challenges", tutorial at 12th IEEE Mediterranean Electrotechnical Conference, MELECON, 2004, May 12-15, Dubrovnik Croatia.

42. M. Hansson, S. Andersson, P. Caputa, A. Alvandpour,"Project and Laboratory Manual for TSEK01, VLSI Design Project. December 2004.