

PUBLICATIONS

Electronic Devices 2001

1. Edman, J. Christensen, A. Emrich, and C. Svensson: "A low-power 416-lag 1.5-b 0.5-TMAC correlator in 0.6 μ m CMOS", IEEE Journal of Solid-State Circuits, Vol. 36, pp. 258–265, Feb. 2001.
2. F. Mu and C. Svensson: "Self-tested self-synchronization circuit for mesochronous clocking", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 48, pp. 129 –140, Feb. 2001.
3. J. Eklund and C. Svensson: "Influence of metastability errors on SNR in successive-approximation A/D converters", Analog Integrated Circuits and Signal Processing, Vol. 26, pp.191-198, Mar. 2001.
4. Rantzer, H. Arwin, J. Birch, B. Hjörvarsson, J.W.P. Bakker, and K. Järrendahl: "Optical properties of intrinsic and doped a-Si:H films grown by d.c. magnetron sputter deposition", Thin Solid Films 394, pp. 256-263, 2001.
5. Svensson and G.E. Dermer: "Time domain modeling of lossy interconnects", IEEE Transactions on Advanced Packaging, Vol. 24, pp. 191 -196, May 2001.
6. Svensson: "Optimum voltage swing on on-chip and off-chip interconnect", IEEE Journal of Solid-State Circuits, Vol. 36, pp. 1108 -1112, Jul 2001.
7. H. Bengtsson and C. Svensson: "3V CMOS 0.35u transimpedance receiver for optical applications". The 2001 IEEE International Symposium on Circuits and Systems, ISCAS 2001, Vol. 5, pp. 455-458, 6-9 May 2001.
8. M. Duppils: "Challenges in analog VLSI", Proc. of Third Conference on Computer Science and Systems Engineering in Linköping, pp. 249-252, Norrköping, Mar. 14-15 2001.
9. D. Eckerbert and P. Larsson-Edefors: "Cycle-True Leakage Current Modeling for CMOS Gates", Proc. of IEEE International Symposium on Circuits and Systems, pp. V 507-510, Sydney, Australia, May 6-9 2001.
10. D. Eckerbert and P. Larsson-Edefors: "Interconnect-Driven Short-Circuit Power Modeling": Proc. of Euromicro Symposium on Digital Systems Design, pp. 414-421, Warsaw, Poland, Sept 4-9 2001.
11. H. Eriksson, P. Larsson-Edefors, and A. Alvandpour: "A 2.8 ns 30 uW/MHz Area-Efficient 32-b Manchester Carry-Bypass Adder", Proc. of the 2001 IEEE International Symposium on Circuits and Systems, pp. IV 84-87, Sydney, Australia, May 6-9 2001.
12. H. Eriksson, P. Larsson-Edefors, and W.P. Marnane: "A Regular Parallel Multiplier which utilizes Multiple Carry-Propagate Adders", Proc. of the 2001 IEEE International Symposium on Circuits and Systems, pp. IV 166-169, Sydney, Australia, May 6-9 2001.
13. K. Folkesson and C. Svensson: "Low-Jitter Clock Paths", the Swedish National Symposium on GigaHerz Electronics, Nov 26-27 2001.
14. K. Folkesson, C. Svensson, and J-E- Eklund: "Modeling of Dynamic Errors in Algorithmic A/D Converters", Proc. of the 2001 IEEE International Symposium on Circuits and Systems, ISCAS 2001, Vol. 5, pp. 455-458, Sydney, Australia, May 6-9 2001.
15. Gustafsson, K. Folkesson, and H. Olsson: "A Simulation Environment for Integrated Frequency and Time Domain Simulations of a Radar Receiver", the Swedish National Symposium on GigaHerz Electronics, Nov 26-27 2001.
16. (D. Jakonis and C. Svensson: "A 1 GHz linearized CMOS track-and-hold circuit", submitted to ISCAS.)

17. P. Larsson-Edefors, H. Eriksson, D. Eckerbert, and A. Alvandpour: "Low-Power Design of Delay-Constrained Circuits using Dual-VT Process Technolog, Proc. of International Workshop on Power and Timing Modeling, Optimization, pp. 7.1.1-10, Yverdon-les-bains, Switzerland, Sept 26-28, 2001.
18. U. Nordqvist: "On protocol processing": Proc. of Third Conference on Computer Science and Systems Engineering, pp. 83-89, Norrköping, Mar.14-15 2001.
19. H. Eriksson: "Glitch-power analysis and power-efficient design of CMOS circuits", Linköping Studies in Science and Technology, Licentiate Thesis 874, ISBN 91-7219-993-8, Mar. 2001.
20. S. Andersson: "Introduction to VLSI – Spice lab", laboratory exercise manual in TSEK30 Introduction to VLSI, undergraduate course 2001.
21. P. Caputa and K. Folkesson: "TFYY64 Advanced VLSI Design – AnalogLab", laboratory manual in Advanced VLSI Design, undergraduate course 2001.
22. P. Caputa and K. Folkesson: "TFYY64 Advanced VLSI Design – WireLab", laboratory manual in Advanced VLSI Design , undergraduate course 2001.
23. P. Caputa and K. Folkesson: "TFYY64 Advanced VLSI Design – MeasurementLab", laboratory manual in Advanced VLSI Design, undergraduate course 2001.
24. H. Eriksson et al: "VLSI Design 2001", laboratory manual in TFFY90 VLSI Construction, undergraduate course 2001.
25. P. Larsson-Edefors: "LedLab: "Layout and verification of a bitcell for a counter", laboratory manual for TFYY62-Introduction to VLSI. Edited by Peter Caputa, 2001.
26. D. Wiklund and S. Andersson: "Introduction to VLSI – Measurement lab", laboratory exercise manual in TSEK30 Introduction to VLSI. undergraduate course 2001.
27. J. Elbornsson, K. Folkesson, and J.-E. Eklund: "Measurement Verification of Estimation Method for Time Errors in a Time-Interleaved A/D Converter Sysstem", submitted.
28. K. Folkesson and C. Svensson: "A Matlab-Based ADC Model for RF System Simulations", submitted.
29. H. Eriksson and P. Larsson-Edefors: "Fast Full Adder Cells with Optimized Carry Circuitry", submitted.
30. M. Drazdziulis, P. Larsson-Edefors, and H. Eriksson: "An Implementation of Signed Booth-Encoded 8x8-bit Regular Reduction Tree Multiplier", submitted.