Brief overview and examples of research work

Division of Integrated Circuits and Systems
Department of Electrical Engineering

About 30 years research experience in integrated circuits and systems design.

Internationally recognized as one of the forerunners in high-speed, low power CMOS circuits and signal processing techniques (in most course books).

Several techniques and concepts utilized in commercial products such as advanced microprocessors, wireless sensors, internet routers, CMOS cameras, data acquisition systems, and more.

Strong tradition of collaboration with industry and academia worldwide.

Produced about 8 full Professors, and more than 60 PhDs who are currently with European and U.S. companies, such as Ericsson, SAAB, Infineon, Intel, Broadcom, NXP, etc.

State-of-the-art laboratories and IC design environment.

Provide broad education including about 20 courses at basic and advance levels within digital, analog, and radio frequency integrated circuits and systems.
Research – Efficient analog, digital, and radio frequency integrated circuits and systems

Mixed Analog/Digital
• Data converters (ADCs and DACs) for high data-rate communications, low-power sensors, and medical implant devices.
• High-precision analog readout and data acquisition for image sensors and other massive parallel sensors.
• Integrated power management systems and power converters for energy harvesting.
• On-chip clock generators, frequency synthesizers, and timing/synchronization.
• High-speed on-chip/off-chip communication links and I/O interface.

Digital
• High-performance and low-power integrated digital processing circuits and systems.
• On-chip networks and on-chip memories.

Radio Frequency (RF) IC
• Energy-efficient RF CMOS power amplifiers and radio transmitter front-ends.
• Flexible RF sampling receiver front-ends for software defined radio.
• Low-power wireless transceivers for wireless sensors.
Examples of IC design projects and results

* The material will be updated every year to include new examples of the ongoing projects and our latest published research work.
Examples of IC design projects and results

Efficient Data Converters (ADCs and DACs)
A 53-nW 9.12-ENOB 1-kS/s SAR ADC in 130 nm CMOS for medical implant devices, particularly for pacemakers

Lowest reported power consumption (53 nW) in 2012 for ADCs for such applications!

A 3-nW 9.1-ENOB SAR ADC at 0.7 V and 1 kS/s in 65nm CMOS, for medical implant devices and ultra-low-power sensors.

D. Zhang, A. Alvandpour, "A 3-nW 9.1-ENOB SAR ADC at 0.7 V and 1 kS/s", in proceedings of the European Solid-State Circuit Conference (ESSCIRC), pp.369-372, Bordeaux, France, September 2012

Lowest reported power consumption of 3 nW, pushed the power limits in 2012, as compared to previously lowest reported power, also from us (in previous slide)
Low-Power ADC DT $\Delta \Sigma$ modulators using SC passive (OTA-less) filters in 65nm CMOS

Active filters in both stages ($\Delta \Sigma_{AA}$)

Passive filter in 2nd stage ($\Delta \Sigma_{AP}$)

Passive filter in both stages (OTA-less modulator, $\Delta \Sigma_{AP}$)

<table>
<thead>
<tr>
<th></th>
<th>$\Delta \Sigma_{AA}$</th>
<th>$\Delta \Sigma_{AP}$</th>
<th>$\Delta \Sigma_{PP}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>fP7M 65nm CMOS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>0.9-V</td>
<td>0.9-V / 0.7-V</td>
<td></td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>250-kHz</td>
<td>500-kHz</td>
<td></td>
</tr>
<tr>
<td>Signal BW</td>
<td></td>
<td>500-Hz</td>
<td></td>
</tr>
<tr>
<td>Peak SNR</td>
<td>80 dB</td>
<td>73.5 dB</td>
<td>70.2 dB / 68 dB</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>76 dB</td>
<td>70 dB</td>
<td>67 dB / 65 dB</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>75 dB</td>
<td>70.5 dB</td>
<td>55 dB / 53 dB</td>
</tr>
<tr>
<td>Power</td>
<td>2.1 $\mu$W</td>
<td>1.27 $\mu$W</td>
<td>0.92 $\mu$W / 0.43 $\mu$W</td>
</tr>
<tr>
<td>Active Area mm$^2$</td>
<td>0.033</td>
<td>0.059</td>
<td>0.125</td>
</tr>
<tr>
<td>FOM$_W$ pJ/step</td>
<td>0.407</td>
<td>0.491</td>
<td>0.503 / 0.296</td>
</tr>
</tbody>
</table>


Division of Integrated Circuits and Systems, Dept. of Electrical Engineering, Linköping University
A compact 16-bit ADC for infrared readout IC

- Utilized in a column-parallel readout structure
- Compact architecture and shared circuitry allows individual channels fit in a 25-μm pitch
- Chopper stabilization reduces offset and 1/f noise

<table>
<thead>
<tr>
<th>Process</th>
<th>0.35 μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample Rate</td>
<td>23.32 kHz (60 fps)</td>
</tr>
<tr>
<td>SNDR</td>
<td>86 dB</td>
</tr>
<tr>
<td>THD</td>
<td>-96 dB</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>90 dB</td>
</tr>
<tr>
<td>- ADC Channel power</td>
<td>570 μW</td>
</tr>
<tr>
<td>- Common Circuitry</td>
<td>24 mW (292 channels)</td>
</tr>
<tr>
<td>ADC Channel</td>
<td>0.018 mm² (25x720 μm)</td>
</tr>
</tbody>
</table>

A Vernier time-to-digital converter with delay latch chain architecture

Synthesizable all-digital ADCs

Example: A time-mode ADC in 65nm CMOS using standard cells

- Signal represented and processed in time instead of voltage/current.
- Ring VCO based noise-shaping, all-digital
- Exclusive use of vendor supplied standard cells
- Spurious-error mitigation using Gray-counter based phase accumulation
- Lowest reported power consumption and best FoM in class

Energy-efficient high-speed Flash ADCs

Example: A low-power 4-bit, 1.5 to 2.5 GHz Flash ADC in 90nm CMOS

- Redundancy-based flash ADC, 63 small-sized comparators for 4-6 bits of resolution.
- Calibration by disabling bad comparators
- The ADC utilizes native mismatches (process variations) and redundancy to generate the references voltages without using reference ladder.

<table>
<thead>
<tr>
<th>Author Year</th>
<th>ENOB</th>
<th>Sampling Freq.</th>
<th>CMOS Process</th>
<th>Power</th>
<th>FoM pJ/Conv-Step</th>
</tr>
</thead>
<tbody>
<tr>
<td>Park, 2007</td>
<td>3.9</td>
<td>4 GS/s</td>
<td>0.18µm</td>
<td>608 mW</td>
<td>20.4</td>
</tr>
<tr>
<td>Park, 2005</td>
<td>5.5</td>
<td>2 GS/s</td>
<td>0.18µm</td>
<td>145 mW</td>
<td>6.41</td>
</tr>
<tr>
<td>Sheikhaei, 2007</td>
<td>3.2</td>
<td>3.0 GS/s</td>
<td>0.18µm</td>
<td>43 mW</td>
<td>1.51</td>
</tr>
<tr>
<td>Deguchi, 2007</td>
<td>4.9</td>
<td>3.5 GS/s</td>
<td>90nm</td>
<td>98 mW</td>
<td>0.95</td>
</tr>
<tr>
<td>Lin, 2007</td>
<td>4.2</td>
<td>4.2 GS/s</td>
<td>0.13µm</td>
<td>180 mW</td>
<td>2.80</td>
</tr>
<tr>
<td>Van der Plas, 2007</td>
<td>3.7</td>
<td>1.25 GS/s</td>
<td>90 nm</td>
<td>2.5 mW</td>
<td>0.15</td>
</tr>
<tr>
<td>Proposed Flash ADC</td>
<td>3.9</td>
<td>2.5 GS/s</td>
<td>90nm</td>
<td>30 mW</td>
<td>3.15</td>
</tr>
<tr>
<td>Proposed reference-free Flash ADC</td>
<td>3.7</td>
<td>1.5 GS/s</td>
<td>90nm</td>
<td>23 mW</td>
<td>1.47</td>
</tr>
</tbody>
</table>


High-speed pipeline ADCs for wideband communications

Example:
A 2.4 GS/s, Single-Channel, 31.3 dB SNDR at Nyquist, 8-bit Pipeline ADC in 65nm CMOS

- Clocking scheme removes the comparator latency from the critical path.
- Fast open-loop amplifiers
- Digital calibration, corrects for stage gain-error and input-stage non-linearity.

### Table: Performance Comparison

<table>
<thead>
<tr>
<th>Author</th>
<th>Year</th>
<th>Architecture</th>
<th>CMOS Process</th>
<th>Sample Rate (GS/s)</th>
<th>ENOB(_{\text{min}}) DC-Nyquist</th>
<th>Power (mW)</th>
<th>FoM (pJ/conv-step)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shen</td>
<td>JSSC-07</td>
<td>Pipeline</td>
<td>0.18µm</td>
<td>0.8</td>
<td>4.9</td>
<td>105</td>
<td>3.3</td>
</tr>
<tr>
<td>Varzaghani</td>
<td>JSSC-09</td>
<td>Interleaved Pipeline</td>
<td>0.13µm</td>
<td>4.8</td>
<td>4.7</td>
<td>300</td>
<td>2.3</td>
</tr>
<tr>
<td>Nazemi</td>
<td>VLSI-08</td>
<td>Interleaved Pipeline</td>
<td>90nm</td>
<td>10.3</td>
<td>5.1</td>
<td>1600</td>
<td>2.8</td>
</tr>
<tr>
<td>This Work</td>
<td></td>
<td>Pipeline</td>
<td>65nm</td>
<td>2.0</td>
<td>5.3</td>
<td>294</td>
<td>2.7</td>
</tr>
</tbody>
</table>

Fastest reported CMOS pipeline ADC in 2011

An 8-GS/s 200-MHz bandwidth 68-mW ΔΣ DAC in 65-nm CMOS for wideband radio transmitters

8GS/s at 200 MHz BW
57dB IM3, 48dB SFDR, 26dB SNDR.
68mW power consumption.

1.5X higher sampling rate and 2X higher bandwidth, compared to previously reported ΔΣ DACs.

Examples of IC design projects and results

Wireless sensors
Ultra Low Power Wake-Up Radio using Envelope Detector and T-Line Voltage Transformer

Utilized in an industrial application for automatic toll collection.

<table>
<thead>
<tr>
<th>Technology</th>
<th>CMOS 180nm</th>
<th>BAW match, CMOS 90nm</th>
<th>BAW match, CMOS 90nm</th>
<th>Off-chip ind., CMOS 90nm</th>
<th>Schottky, μCtrl</th>
<th>Schottky, μCtrl</th>
<th>CMOS 180nm</th>
<th>FR4 match, CMOS 130nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency [MHz]</td>
<td>2400</td>
<td>1900</td>
<td>2000</td>
<td>2400</td>
<td>868</td>
<td>860</td>
<td>2400</td>
<td>2450</td>
</tr>
<tr>
<td>nJ/bit</td>
<td>0.86</td>
<td>1.6</td>
<td>0.52</td>
<td>0.51</td>
<td>1350</td>
<td>-</td>
<td>0.55</td>
<td>0.023</td>
</tr>
<tr>
<td>Bit rate [kbps]</td>
<td>250</td>
<td>40</td>
<td>100</td>
<td>100</td>
<td>0.75</td>
<td>9.6</td>
<td>1.95</td>
<td>200</td>
</tr>
<tr>
<td>Sensitivity [dBm]</td>
<td>-86</td>
<td>-50</td>
<td>-72</td>
<td>-64</td>
<td>4.37</td>
<td>-35</td>
<td>-29.8</td>
<td>-47</td>
</tr>
<tr>
<td>Power [μW]</td>
<td>215</td>
<td>65</td>
<td>52</td>
<td>51</td>
<td>12.5</td>
<td>10.8</td>
<td>1.08</td>
<td>2.3</td>
</tr>
</tbody>
</table>

Analog receiver front-end for body-coupled communication

- Power consumption of full AFE < 10 mW
- Integrated in printed electronics labels (Tx) and mobile phones (Rx)
- ID exchange and handshaking

I. Kazim, JJ Wikner, “An analog receiver front-end for capacitive body-coupled communication”, in IEEE NorChip 2012, pp 1-4
Examples of IC design projects and results

Integrated sensor readout and data acquisition ICs
Readout IC for an uncooled FPA infrared network camera

- 288 X 288 Infrared sensor array.
- Column parallel readout with 288 15-bit compact ADCs in 25-μm pitch!

A high-rate energy-resolving photon-counting ASIC for spectral computed tomography

In cooperation with Royal Institute of Technology, Stockholm

<table>
<thead>
<tr>
<th>Specification</th>
<th>Target/Simulation</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of channels</td>
<td>160</td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td>2.08mV/keV</td>
<td>2.10mV/keV</td>
</tr>
<tr>
<td>Noise level, ENC</td>
<td>300 electrons @5pF</td>
<td>207 electrons @-4pF, 40ns</td>
</tr>
<tr>
<td>Number of energy bins</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Energy bin counter resolution</td>
<td>8b</td>
<td></td>
</tr>
<tr>
<td>Peak times</td>
<td>10ns, 20ns, 40ns</td>
<td>10ns, 20ns, 40ns</td>
</tr>
<tr>
<td>Maximum count rate</td>
<td>17Mcps @100MHz clock</td>
<td>17Mcps @100MHz clock</td>
</tr>
<tr>
<td>Maximum frame rate</td>
<td>38kframes/s @100MHz clock</td>
<td></td>
</tr>
<tr>
<td>Clock frequency</td>
<td>100MHz, 200MHz</td>
<td>100MHz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>800mW @ 200MHz clock</td>
<td>670mW @ 100MHz clock</td>
</tr>
<tr>
<td>Chip area</td>
<td>5mm x 6.6mm</td>
<td></td>
</tr>
</tbody>
</table>

Process: 180nm CMOS
1.6 Million transistors

Examples of IC design projects and results

Efficient radio transceiver front-ends
Innovative wideband Class-D outphasing radio power amplifiers

Example 1:

A +32dBm 1.85GHz Class-D Outphasing RF PA in 130nm CMOS for WCDMA/LTE

RF Performance

- $P_{out} = +32$ dBm,
- DE = 20.1%, PAE = 15.3%
- 3dB bandwidth: 0.9 GHz (1.2-2.1 GHz)
- WCDMA (5 MHz)
- PAPR = 3.5dB
- Channel Power: +28dBm
- LTE (20 MHz, 16-QAM)
- PAPR = 6.6dB
- Channel power: +24.9dBm
- No predistortion used

Highest reported output power (32 dBm) for CMOS outphasing PAs in 2011!

Innovative wideband Class-D outphasing radio power amplifiers

Example 2:

A Wideband Fully Integrated +30dBm Class-D Outphasing RF PA in 65nm CMOS

RF Performance:

- $P_{out} = +29.7$dBm
- DE = 30.2%, PAE = 26.6%
- 3dB bandwidth: 1.6GHz (1.2-2.8GHz)
- WCDMA @ 5 MHz
- PAPR = 3.5dB
- Channel Power: +26dBm
- LTE (20 MHz, 16-QAM)
- PAPR = 6.6dB
- Channel power: +22.9dBm
- No predistortion was used

Among highest reported bandwidth (1.6 GHz) for CMOS outphasing PAs

Innovative predistortion methods for Class-D outphasing PAs, supporting high linearity requirements for radio base-stations

Example:
Least-squares phase predistortion of Class-D outphasing PA in 65nm

Improved predistortion model from nonconvex to a convex least-squares problem. Predistorter can be calculated analytically.


(a) Measured spectrum without DPD
(b) when DPD is applied to (a)
(c) Spectrum of estimation signal
Low-power fast-hopping DLL-based WiMedia UWB synthesizer

- Process: 65nm CMOS
- Supports band group 1, with -44dBc spur with power consumption of 21mW
- Open-loop VCDL delay compensation
- PVT calibration
- Injection locked edge combiner

Efficient modeling and analysis of harmonic spurs in DLL-based frequency synthesizers

Proposed analytical expressions simplify the design process of DLL-based frequency synthesizers by removing the need for exhaustive Monte-Carlo simulations!


Radio receiver frontends with high blocker rejection capability

Example:
A two-stage highly selective receiver front-end based on impedance transformation filtering.

Front-end Architecture | Zero-IF
---|---
Technology | 65 nm
System | Front-end
Frequency [GHz] | 0.5 – 3
Gain [dB] | 45 – 25
NF [dB] | 3.2 – 5.3
NF@0dBm blocker [dB] | 12@100 MHz offset for 2 GHz LO
Blocker Rejection | 60- 38 dB
Out-of-band IIP3@100MHz [dBm] | +20
Blocker P1dB@100MHz [dBm] | +5
Power Consumption [mW] | 46 – 113
Chip area [mm²] | 1.7

Flexible radio sampling receiver front-ends

A 2.4-GHz RF Sampling Receiver Front-End in 0.18-μm CMOS

- Constellation diagram for a 64 QAM modulated WLAN signal. EVM = 7% RMS (54 Mb/sec)

One of the first reported flexible radio sampling receiver front-end for software defined radio

- Technology: 0.13um CMOS
- Voltage Gain: 17 dB
- Frequency range: 1-7 GHz
- NF: 2.4 dB at 3 GHz
- IIP3: -4.1 dBm
- 1dB CP: -20 dBm
- Power, at 1.4V: 25 mW
- Active Area: 0.019 mm²

D Jakonis, K Folkesson, J Dabrowski, P Eriksson and C Svensson, “A 2.4-GHz RF Sampling Receiver Front-End in 0.18-μm CMOS”. In IEEE Journal of Solid-Stated Circuits, Vol 40, No 6, June 2005, pp 1265-1277.

A 1.4V, 25mW inductor-less wideband LNA in 0.13μm CMOS

Examples of IC design projects and results

Example of earlier work on high-speed digital building blocks, memories, on/off-chip communication/synchronization and clock generators
2.6 Gb/s, 93mA, 12 tap 8 bit equalizer receiver for multi-drop DRAM memory bus

Adaptive 12 tap 8 bit single ended Decision Feedback Equalizer (DFE) receiver and BER measurement circuits in 130nm CMOS, 1.2V.

Total equalizer area: 0.187 mm²

Synchronous latency insensitive on-chip communication

0.18µm CMOS

A 2GHz 7mW digital DLL-based frequency multiplier in 90nm CMOS

Process: 90-nm CMOS
Area: 0.037 mm²
Power: 7 mW at 2 GHz
(6.75 mW DLL, and 0.25 mW FM)
Jitter: rms = 1.6 ps, and p-p = 9.5 ps
14% power reduction compared to previously reported works.

First reported ‘buffer-less’ resonant clock distribution, with up to 70% power saving

Process: 130nm CMOS
Area: 1.48 X 2.18mm

Clock Frequency: up to 1.8 GHz
29ps p-p jitter at 1.56 GHz
57%-73% lower clock power

A high density, low leakage, 5T SRAM for embedded caches

Process: 0.18μm CMOS
Cell area (with logic design rule): 6.30μm² (7.99μm² for 6T)
Memory area: 0.88mm²

Comparison to conventional 6T cell SRAM:
- 40% lower cell leakage
- 70% smaller bitline leakage
- 22% smaller area
- Comparable read/write performance

Full read/write functionality for all 128K 5T-cells
Total read delay of 360ps.


Also in Intl. Conference on Memory Technology and Design (ICMTD 07), pp. 185-188, Giens, France, 2007
Contributions to Intel 80 core teraflop processor

- Sustained 1.01 Teraflops at 97 watts (65nm CMOS)
- Measured power efficiency of 19.4 GFLOPS/Watt

S. Vangal, A. Singh, J. Howard, S. Dighe, N. Borkar, and A. Alvandpour, "A 5.1 GHz 0.34 mm² Router for Network-on-Chip Applications", 2007 Symposium on VLSI Circuits, pp. 42-43, Kyoto, Japan, 2007


Teraflop 80-Core Programmable Processor

What's your soft

Sony Ericss

Datorer

PUBLICERAD 070313, 16:46
Intels nya superchip föddes i Linköping

Processorn är uppbyggd kring en krets med 80 processorkärnor, inte större än en fingernagel. Den har kapaciteten drygt 1 teraflop, men förbrukar trots det bara 0,2 watt. Det är mindre än vad många av dagens pc-processorer med betydligt benödvandigare förbrukar.

Dr. Ake Hjelm

Arbetet med teraflop-processorn beskrivs i Striram Vangals 60-sta licentiatavhandling från Litu 2006. Resultatet av hans forskning tillsammans med professor Attila Alvandpour har också publicerats i flera vetenskapliga artiklar, skriver Litu-reportern Ake Hjelm.
Thank you

For further information about our research and education or in case of interest in future collaboration, please don't hesitate to contact us.

Regards

Atila Alvandpour, Professor, Division Head
Email: Atila.Alvandpour@Liu.se